

Serial No.: 10/808,341  
Docket No.: 101-1019  
Amendment dated May 17, 2007  
Reply to the Final Office Action of March 21, 2007

## **REMARKS**

### **Introduction**

Upon entry of the foregoing amendment, claims 1-27 are pending in the application. Claims 7-10 and 19-27 have been withdrawn. Claims 11 and 17 have been allowed. Claims 1, 12, 14, 15 and 18 have been amended and claims 28-33 have been added. No new matter is being presented. In view of the following remarks, reconsideration and allowance of all the pending claims are requested.

### **Objections**

Claim 1 has been objected to due to a misspelling of the word "eighth." Accordingly, the spelling error has been corrected not only in claim 1, but in claims 14 and 15, as well.

### **Rejection under 35 USC §101**

Claim 18 has been rejected under 35 U.S.C. §101 as reciting subject matter directed to an apparatus and a method in a single claim. Accordingly, claim 18 has been amended to recite structure to implement the interoperation of its member components.

### **Rejection under 35 USC §112**

Claim 12 has been rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner stated that the recitation of "the at least three memory devices in the first and third rows" is unclear as to which devices are being referred to. Accordingly, claim 12 has been amended and now unambiguously recites the limitations thereof.

Claim 18 has been rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The Examiner stated that the claim, as originally presented, was directed to both an apparatus and method step and that it would be unclear, if allowed, whether infringement occurs when the apparatus is created or when it is actually put to use. The amendments to claim 18 include clarifications to the recited structure and the subject claim is now unambiguous in its recitations.

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### **Rejection under 35 USC §102**

Claims 12-16 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Publication No. 2003/0007636 to Alves, et al. (hereinafter "Alves"). Applicants respectfully traverse the rejections of the subject claims for at least the reasons discussed below.

#### **Claim 12**

In setting forth the rejection of the subject claim, the Examiner takes the position that decoder 220 in figure 2 of Alves corresponds with the first communication port recited in claim 12. Additionally, the Examiner relies on figure 1 to allegedly show correspondence thereof with elements recited in the subject claim and asserts that "there are multiple I/O connections between 106 and 112, 110, and 120," where 112, 110 and 120 memory circuits outside the processing element (PE) array 106. The Examiner further alleges that the reconfigurable cell (RC) element of Alves corresponds to the calculation element recited in claim 12 when the RC is one position in the PE array and corresponds to memory units recited in the subject claim when the RC is in other positions in the array. To this point, the Examiner contends that "each RC comprises functional units, i.e. calculation elements, and memory."

Prior to discussing the merits of Alves as a basis for a rejection of claim 12 under 35 U.S.C. § 102, it is respectfully submitted that, whereas the Examiner is rightly required to give the claims "their broadest reasonable interpretation consistent with the specification," (the Federal Circuit's *en banc* decision in Phillips v. AWH Corp., 415 F.3d 103, 75 USPQ2d 1321 (Fed. Cir. 2005)), "the words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification." In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). In view of the Examiner's reasoning behind the rejection of the subject claim, it is undeniable that the Examiner has not given plain meaning to the term "directly connected" in the recitation of "the calculation element is surrounded by the ... memory devices and is directly connected with each of the ... memory devices," (emphasis added) in claim 12 when applying Alves thereto. Indeed, even a cursory review of FIG. 3 of Alves reveals that a neighboring RC can only access any of the limited memory of another RC through numerous processing elements, which precludes a processing element in an RC to be "directly connected with...memory devices." Moreover, the fact that memory in an RC of Alves is

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interposed between data processing elements of the RC is also demonstrative that the RC of Alves as a unit cannot serve as a "memory device," when that term is given its plain meaning, also.

As the Examiner is aware, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as contained in the...claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Moreover, "The elements must be arranged as required by the claim..." *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Thus, for at least the reason that Alves fails to disclose or teach "the calculation element is surrounded by the ... memory devices and is directly connected with each of the ... memory devices," as recited in independent claim 12, the reference cannot anticipate this claim. Accordingly, withdrawal of the rejection and allowance of independent claim 12 are earnestly solicited.

It is respectfully submitted, also, that the Examiner has failed to address how Alves allegedly discloses "at least three memory devices connected with the first communication port and arranged in a first row direction of the DSP architecture" and "at least three memory devices connected with the first communication port and arranged in a third row direction of the DSP architecture." In the Official Action, at paragraph 9, the Examiner contends that "all elements are connected to all other elements and ports, i.e., there is a connection to any port through any element." However, it is respectfully submitted that, if by the ambiguous references to "all elements" and "any elements," the Examiner is referring to individual components within each RC, which must be assumed if the Examiner is attempting to apply Alves to the recitations of the subject claim, then the Examiner has erred as there no evidence in Alves that a connection between elements so defined is contemplated. Clearly, decoders 220 and 230 in Alves are specified to addressing individual RCs in the rows and columns of the array 106. Thus, the decoders 220 and 230 clearly function in Alves as an addressing mechanism (see Alves, paragraph [0016], starting at line 9 thereof), and not a "communication port" as defined in the specification of the subject patent application, i.e., "the data input to the first communication port 501 is stored in the memories..." (see paragraph [0033] of the subject patent application).

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Nowhere is it taught in the reference where a decoder 220 is connected to memory internal to an RC and, even if this point were to be disregarded, there is no teaching in Alves to suggest that data are transferred into memory within an RC by way of the decoders 220 and 230. If, however, the Examiner is relying on some inherent feature of the RC, the decoder 220, or the connection therebetween, then "the Examiner must provide a technical basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990; emphasis in original). The Examiner's reasoning that "memory devices connected with the first communication port," as recited in claim 12, is met by Alves since, allegedly, "106 has multiple I/O ports" and "all elements are connected to all other elements and ports," is insufficient to properly establish anticipation, because what is at issue is "[the] elements [being] arranged as required by the claim." And, in light of the arguments set forth above, Alves unquestionably fails to show each and every element in the arrangement recited in independent claim 12, and for at least this reason, the reference cannot anticipate this claim. Accordingly, withdrawal of the rejection and allowance of independent claim 12 are earnestly solicited.

#### Claim 13

Dependent claim 13 incorporates all of the limitations set forth in independent claim 12. For at least the same reason that Alves does not disclose or teach all of the elements set forth in independent claims 12, it is respectfully submitted that claim 13 is not anticipated by the reference. Accordingly, withdrawal of the rejection and allowance of this claims are earnestly solicited.

#### Claim 14

Independent claim 14 recites elements in common with elements recited in independent claim 12. Thus, for at least the same reasons that the common elements are not disclosed or taught by Alves, as discussed above with reference to claim 12, the reference cannot anticipate independent claim 14. Accordingly, for at least this reason, withdrawal of the rejection and allowance of independent claim 14 are earnestly solicited.

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Additionally, however, the Examiner has failed to address how Alves allegedly discloses "first through eighth memories to store respective ones of the image frames of the first and second motion picture image data," as recited in independent claim 14. In that the Examiner is apparently attempting to equate unspecified memory in several RCs as each of the "first through eighth memories", it is to be made clear that nowhere in Alves is it disclosed or taught that memory internal to an RC is capable of storing an entire frame of image data. Whereas the Examiner asserts in paragraph 14 of the Official Action that "the 'limitations' are phrased using what seems to be a term that denotes intended use. There's nothing to suggest that the digital signal processor disclosed by Alves cannot be used to encipher or decipher motion picture data," the fact remains that there is no memory in an RC, or anywhere else in Alves "to store respective ones of the image frames," were such image frames to be provided thereto. Regardless of whether Alves' system could encipher or decipher motion picture data, as the Examiner alleges, it would still lack the capability "to store respective ones of the image frames," as recited in independent claim 14, including in the memory referred to in Alves as a "frame buffer." See Alves at paragraph [0012]. Thus, for at least this reason, the reference fails to disclose or teach each and every element recited in independent claim 14, and cannot therefore anticipate this claim. Accordingly, withdrawal of the rejection and allowance of the subject claim are earnestly solicited.

It is respectfully submitted that the Examiner appears to be determining anticipation of this and other pending claims through determining the presence or absence in the reference of individual elements recited in the claim without regard to the requirements that "[t]he identical invention must be shown in as complete detail as contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), and that, "[t]he elements must be arranged as required by the claim..." In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Clearly, for independent claim 14 to be anticipated by Alves, then the reference must show "memories to store respective ones of the image frames."

#### Claims 15 and 16

Dependent claims 15 and 16 incorporate all of the limitations set forth in independent claim 14. For at least the same reason that Alves does not disclose or teach all of the elements set forth in independent claim 14, it is respectfully submitted that claims 15 and 16 are not

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anticipated by the reference. Accordingly, withdrawal of these rejections and allowance of these claims are earnestly solicited.

### **Rejection under 35 USC §102**

Claims 1-6 and 12-16 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Publication No. 2003/0220562 to Sasaki et al. (hereinafter "Sasaki"). Applicants respectfully traverse these rejections for at least the reasons discussed below.

#### **Claim 1**

The processing configuration of FIG. 14 in Sasaki, on which the Examiner relies, is very similar to the configuration and functionality of that of Alves and the same shortcomings discussed with regard to Alves are also shortcomings of Sasaki with respect to the recitations of the pending claims. In the interest of brevity, the deficiencies of Sasaki in common with Alves will not be reiterated, with a few exceptions below, but all of the remarks above with regard to Alves' shortcomings as a reference allegedly anticipating claims 12 and 14 apply to describing the shortcomings of Sasaki as a reference allegedly anticipating claims 1, 12 and 14. For at least those common reasons set forth above, Sasaki does not disclose each and every element recited in independent claim 1 (and independent claims 12 and 14) and cannot therefore anticipate the subject claim. Accordingly, for at least this reason, withdrawal of the rejection and allowance of independent claim 1 (and independent claims 12 and 14) are earnestly solicited.

It is respectfully submitted that the Examiner has failed to address how Sasaki allegedly discloses "first, second and third memory devices, which are connected with the first communication port and are arranged in a first row direction of the DSP architecture" and "sixth, seventh, and eighth memory devices, which are connected with the first communication port and are arranged in a third row direction of the DSP architecture." In the Official Action, at paragraph 11, the Examiner takes the position that "each PE has a calculation circuit and a memory circuit" and that "each PE has at least three ports that connect to ports of other PEs; also, although not shown, I/O ports external to the matrix are implicit, if not inherent, as the matrix would be useless without being able to move data in and out of the matrix." To the latter argument, whether each PE has three ports and what, if any, connection exists to external I/O ports, is immaterial to the present patentability analysis. As with the Alves, there is no

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disclosure in Sasaki of a "first communication port", as defined in the specification of the subject patent application, and, as such, the "memory devices, which are connected with the first communication port" are also not shown in the reference. Regardless of whether the PEs of Sasaki provide some communication between the processing elements to implement a distributed processing device, as stated above with regard to Alves, anticipation requires that the claimed structure, arranged as recited in the subject claim, must be shown in the reference. The provision of I/O ports external to a processing matrix, well known though it may be, is not evidence of the reference disclosing "first, second, and third memory devices, which are connected with the first communication port and are arranged in a first row direction of the DSP architecture" and "sixth, seventh, and eighth memory devices, which are connected with the first communication port and arranged in a third row direction of the DSP architecture," which it clearly does not. And, as discussed with regard to Alves, if the Examiner is relying on some inherent feature of the PE of Sasaki, then "the Examiner must provide a technical basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990; emphasis in original). Although the Examiner seems to believe that since each PE of Sasaki has three ports that connect with ports of other PEs, that one should assume as an inherent or implicit feature of the cited system that a single communication port is connected to first, second and third memory devices and to sixth, seventh and eighth memory devices. Such an interconnection cannot be automatically assumed as an inherent feature of Sasaki. And, for at least the reason that Sasaki fails to show each and every element in the arrangement recited in independent claim 1, the reference cannot anticipate this claim. Accordingly, withdrawal of the rejection and allowance of independent claim 1 are earnestly solicited.

In the official action, the Examiner also relies on the PE of Sasaki as having a calculation circuit and a memory circuit, apparently to draw correspondence between the alleged memory feature in the PE as one of the first through the eighth memory devices recited in claim 1 and then to cite the calculation circuit in a center PE as corresponding to the calculation element recited in independent claim 1. Indeed, in the Official Action at paragraph 15, the Examiner asserts that "figure 18 (as evidence) [shows] that Sasaki explicitly shows what is implicit, if not

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inherent, in every PE - that a processing element comprises memory elements, and therefore, the PE reads on the 'memory device' limitation." However, for the same reasons discussed with regard to Alves, the structural elements recited in claim 1, in the arrangement and interconnection defined in the claim, are not disclosed or taught by Sasaki. Thus, for at least these reasons, Sasaki cannot anticipate the claim and withdrawal of the rejection and allowance of independent claim 1 are earnestly solicited.

#### Claims 2-6

Dependent claims 2-6 incorporate all of the limitations set forth in independent claim 1. For at least the same reason that Sasaki does not disclose or teach all of the elements set forth in independent claim 1, it is respectfully submitted that claims 2-6 are not anticipated by the reference. Accordingly, withdrawal of these rejections and allowance of these claims are earnestly solicited.

#### Claim 12 and 14

Claims 12 and 14 recite common elements with elements recited in Claim 1. Thus, for at least the same reasons that the common elements are not disclosed or taught by Sasaki, as discussed above with reference to claim 1, the reference cannot anticipate this claim. Moreover, Sasaki fails to disclose or teach the recited features of claims 12 and 14 for at least the same reasons for which Alves fails to disclose these features. Accordingly, for at least these reason, Sasaki cannot anticipate claims 12 and 14. Accordingly, withdrawal of the rejections and allowance of independent claims 12 and 14 are earnestly solicited.

#### Claims 15 and 16

Dependent claims 13, 15 and 16 incorporate all of the limitations set forth in independent claims 12 and 14. For at least the same reason that Sasaki does not disclose or teach all of the elements set forth in independent claims 12 and 14, it is respectfully submitted that claims 13, and 15-16, respectively, are not anticipated by the reference. Accordingly, withdrawal of these rejections and allowance of these claims are earnestly solicited.

#### New Claims

Claims 28-33 have been added. No new matter is being introduced and support for the



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new claims can be found throughout the specification, such as, for example, in FIGS. 3, 4 and 6-8, the descriptions thereof, and paragraph [0042].

**Conclusion**

It is respectfully submitted that a full and complete response has been made to the outstanding Office Action and, as such, there being no other objections or rejections, this application is in condition for allowance, and a notice to this effect is earnestly solicited.

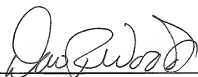
If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided below.

If any further fees are required in connection with the filing of this amendment, please charge the same to our Deposit Account No. 502827.

Respectfully submitted,

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